

PATENT APPLICATION

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**METHOD AND APPARATUS OF
VIDEO GRAPHICS AND AUDIO PROCESSING**

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Technical Field of the Invention

This invention relates generally to computer peripherals and more particularly to graphics processing and audio processing.

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Background of the Invention

Computers are known to include a central processing unit (“CPU”), main memory, system buses, and a plurality of supporting units. Such supporting units include audio processing circuitry, video processing circuitry, graphical user interface modules, etc.

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Physically, many of the supporting units are mounted or coupled to a motherboard. Each of the supporting units, when coupled to the motherboard, includes a local bus that couples the supporting unit to the system bus.

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In operation, when the CPU is inputting, or outputting, data from a supporting unit, it generates an address and a command, which are provided on the system bus. Each of the supporting units, via its local bus, monitors the address bus to determine whether the particular command is directed to it. When the appropriate supporting unit detects that the command is for it, it performs the command. If the command is to input data, the supporting unit stores, and processes –if instructed-, the data provided by the CPU. If the

command is to output data, the supporting unit outputs the data via the local bus to the system bus and routes it either to the CPU, or a designated recipient.

In a typical computer, the video graphics processing circuitry is on a separate board than the audio processing circuitry. As such, the video graphics circuit board and the audio processing circuit board each have their own local buses. In addition, they each require coupling to the motherboard and function as totally independent circuits. A typical audio processing circuit board will retail for approximately \$30.00, which, in turn, relates to approximately \$15.00 of manufacturing costs. With the ever-increasing demand for smaller, more powerful, and less expensive computers, it would be desirable to reduce the cost of including an audio processing circuit.

Therefore, a need exists for a method and apparatus of a graphics circuit and audio processing circuit contained on a single chip and/or printed circuit board.

Brief Description of the Drawing

Figure 1 illustrates a schematic block diagram of a computer system in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of the bus arbitration circuit of Figure 1;

Figure 3 illustrates a schematic block diagram of a video graphics and audio processing circuit in accordance with the present invention;

Figure 4 illustrates a schematic block diagram of an arbitrator in accordance with the present invention; and

Figure 5 illustrates a logic diagram of a method for processing graphics and audio in accordance with the present invention.

Detailed Description of a Preferred Embodiment

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Generally, the present invention provides a method and apparatus for combining video graphics processing and audio processing onto a single chip and/or the same printed circuit board. The combined circuit includes a graphics processing circuit, an audio processing circuit, a local bus, and a bus arbitrator. The local bus couples both the 10 graphics processing circuit and audio processing circuit to the system bus such that each of the circuits may transceive data with the system bus. The bus arbitrator arbitrates access to the local bus between the graphics processing circuit and audio processing circuit. Such arbitration is based on incoming data, which is interpreted and, based on the interpretation, the bus arbitrator routes the incoming data to either the graphics processing circuit or the audio processing circuit. In addition, the bus arbitrator arbitrates outputting 15 data from the graphics processing circuit and the audio processing circuit based on commands received from the CPU. With such a method and apparatus, a single local bus may be used for both the graphics processing circuit and audio processing circuit. By combining the audio processing circuit with the video graphics processing circuit, the 20 costs of adding audio processing to a computer is substantially reduced, since the only cost incurred for adding audio is to include an audio codec and the bus arbitration circuit which is in the \$2.00 to \$3.00 range.

The present invention can be more fully described with reference to Figures 1 through 5. Figure 1 illustrates a schematic block diagram of a computer 10 that includes a 25 CPU 12, a video graphics and audio processing circuit 14, and a system bus 16. The video graphics and audio processing circuit 14 includes a local bus 18, a bus arbitrator 20, an audio processing circuit 22, and a graphics processing circuit 24. The audio processing circuit 22 includes circuitry to process analog audio and digitized audio. Such circuitry

may include a wave table, audio playback circuitry, audio record, a mixer, and an audio codec. The video graphics processing circuit 24 includes circuitry to process analog video and digitized video signals. Such digitized video signals may be generated by the CPU based on software applications, such as a word processing document, graphics document, 5 reading a CD drive. The analog video signals may come from a television encoder that is coupled to receive television broadcasts, cable broadcasts, satellite broadcasts, VCR transmissions and/or DVD transmissions. The video graphics circuit 24 may be equivalent to the video graphics circuit contained in the All-In-Wonder circuit manufactured and distributed by ATI Technologies.

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In operation, the CPU generates commands for inputting and/or outputting data to/from the audio processing circuit and graphics processing circuit. Such commands include an address and an indication as to whether the command is for inputting data, outputting data, and/or processing data. The CPU places the command on the system bus, which is monitored by the bus arbitration circuit 20. When the bus arbitration circuit 20 recognizes the address for either the audio processing circuit 22 or the graphics processing circuit 24, it retrieves the command from the bus. The bus arbitration circuit 20, after interpreting the command, provides the command to either the audio processing circuit 22 or the graphics processing circuit 24. Such an interpretation is based on the address 15 provided by the CPU.

The bus arbitration circuit 20 can be described in greater detail with reference to Figure 2. As shown, the bus arbitration circuit 20 includes an address decoder 30 and an output data switch 32, both of which are coupled to the audio processing circuit 22 and the graphics processing circuit 24. The address decoder 30 includes a data router 34 and control circuitry 36. The output data switch 32 includes a graphics buffer 38, an audio buffer 40, and a multiplexor 42.

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The address decoder 30 is operably coupled to receive addresses 44 and data 46 via the local bus 18. The addresses 44 are provided to the data router 34 and the control circuitry 36. The data router 34 interprets the address 44 to determine whether the received data 46 is for the audio processing circuit 22 or the graphics processing circuit 24. Such an interpretation may be done by a look-up table or other equivalent address matching schemes. Based on the interpretation, the router 34 then acts as a switch to direct the received data 46 to the appropriate circuit 22 or 24.

The control circuitry 36 also interprets the address 44 to provide an enable/disable command signal 54 to the audio processing circuit and the graphics processing circuit 24. For incoming data, or received data 46, the control circuitry 36 generates an enable signal 54 to enable the appropriate circuit 22 or 24 to receive the data. The control circuitry 36 also receives a data command signal 48 from the CPU via the local bus 18. The data command may be a read command, write command, a read and write command, and/or a processing command.

If the data command signal 48 is a write command, the received data 46 is provided to the appropriate circuit 22 or 24 and stored therein. If the data command signal 48 is a read command, the control circuitry 36 provides an enable signal and a read command signal to the appropriate circuit 22 or 24. The appropriate circuit provides an output that is provided to the output data switch 32. In particular, the audio processing circuit 22 produces an audio output data 58, and the graphics processing circuit 24 produces graphics output data 56. If the data command signal 48 is a write-modified read command, the control circuitry provides such an indication via the enable/command signal 54 to the appropriate circuit 22 or 24. The appropriate circuit then writes the data, performs the requested modification, and then provides the data to the output data switch 32.

The output data switch 32 receives the graphics output data 56 into a graphics buffer 38. Similarly, the output data switch 32 receives the audio output data 58 in an audio buffer 40. The graphics buffer 38 and the audio buffer 40 may be first in/first out (“FIFO”) buffers. The output of the buffers are provided to multiplexor 42 which is controlled via an output data control signal 50. The control circuitry 36 generates the output data control signal 50 based on the addresses 44 and the data command signals 48. Based on this control signal 50, the multiplexor 42 outputs data as data output 52.

When the data commands are for the audio processing circuit or the graphics processing circuit 24 only, the data output 52 will be either the graphics output data 56 or the audio output data 58. If, however, multiple data command signals 48 are addressed to both the audio processing circuit and the graphics processing circuit to generate a stream of data, the output data 52 will be graphics output data 56 intermixed with the audio output data 58. This is shown graphically as an intermixed data output signal 52. Thus, by including a bus arbitration circuit, the video graphics processing and audio processing may be combined onto a single chip and/or printed circuit board requiring only a single local bus interface to the system bus and single connector to interface with the mother board. By combining the audio processing and video graphics processing, the cost for including audio processing in a computer is substantially reduced.

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Figure 3 illustrates a schematic block diagram of a video graphics and audio processing circuit 70. The processing circuit 70 includes memory 72 and a processing unit 74. The processing unit 74 may be a micro-processor, microcomputer, microcontroller, digital signal processor, CPU and/or any device which manipulates digital information based on programming instructions. The memory may be random access memory, read-only memory, magnetic tape memory, hard-drive memory, floppy disk memory, CD memory, DVD memory and/or any device that stores digital information.

The memory 72 stores programming instructions that, when read by the processing unit, causes the processing unit to function as a plurality of circuits 76-80. While reading the programming instructions, the processing unit functions as a circuit to receive at least one address and data command. The data command may be for inputting or outputting 5 data from the processing circuit 70. The address will identify either audio processing or video processing. When a plurality of addresses are received, they may be for audio processing, video graphics processing or a combination thereof.

The processing unit 74 further executes programming instructions to function as 10 circuit 78. As circuit 78, the processing unit audio processes the associated data command when the address identifies audio processing. The processing unit 74 also performs programming instructions that cause it to function as circuit 80. At circuit 80, the processing unit 74 graphic processes the associated data command when the address identifies graphic processing. The processing circuit 70 outputs the processed data, 15 whether audio processed or graphics processed, to the system bus via a single local bus. As such, the audio and video graphics processing circuit may be implemented by a single processing unit or a plurality of processing units contained on a single chip and/or printed circuit board that includes a single local bus.

Figure 4 illustrates a schematic block diagram of an arbitrator 90. The arbitrator 20 90 includes memory 92 and a processing unit 94. The processing unit 94 may be a microcomputer, microprocessor, microcontroller, digital signal processor, central processing unit, digital logic control, and/or any other device that manipulates digital information based on programming instructions. The memory 92 may be read-only 25 memory, random access memory, floppy disk memory, hard drive memory, magnetic tape memory, CD ROM memory, DVD memory, and/or any device that stores digital information.

The memory 92 stores programming instructions that, when read by the processing unit 94, causes the processing unit 94 to function as a plurality of circuits 96 and 98.

While performing the programming instructions, the processing unit 94 functions as circuit 96. As circuit 96, the processing unit receives at least one address and determines

- 5 whether the address identifies audio processing or graphics processing. The processing unit then functions as circuit 98 to arbitrate access to a local bus between an audio processing circuit and a graphics processing circuit. The programming instructions performed by the arbitrator 90 will be discussed in greater detail with reference to Figure 5.

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Figure 5 illustrates a logic diagram of a method for arbitrating access to a local bus between a video graphics processing circuit and an audio processing circuit contained on the same single chip and/or printed circuit board. The process begins at step 100 where at least one address and an associated command is received. For each address received, there may be an associated command such that each request of the graphics and audio processing circuit is requesting a different action to be performed. For example, the associated command may be for inputting data (i.e., writing data), outputting data (i.e., reading data) or a write-modify read command.

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If, however, multiple addresses, or at least one, identify both the audio processing and graphics processing to produce a stream of data, the process proceeds to step 108. At step 108 access to the local bus is arbitrated between the audio processing circuit and the graphics processing circuit such that the respective circuits may perform the appropriate command. The arbitration will be based on the number of commands and/or the volume of data being processed by the appropriate circuits. As such, the video graphics circuit will have access to the local bus the majority of the time with the audio processing circuit being intermixed therewith. Such intermixing may be programmable to enhance performance of data throughput.

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The preceding discussion has presented a method and apparatus for video graphics and audio processing being done on a single chip and/or printed circuit board. By integrating video graphics and audio processing onto a single chip and/or printed circuit board, the cost of adding audio processing into a computer is substantially reduced. As previously mentioned, the costs for a separate audio processing board is \$30.00 retail and approximately \$15.00 to manufacture. By integrating the audio processing onto the video graphics board, the cost is reduced to a few dollars of manufacturing cost.

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